



AN110 – EVD1000/1500: Synchronizing to External SYNC Inputs

INTRODUCTION

The EVD1000/1500 has a very flexible digital I/O structure, and in-circuit applications can be configured in a variety of fashions, utilizing different video data formats, levels of user control, etc. It uses horizontal and vertical blanking signals to determine the active area of the video frame on which to perform enhancement. These blanking signals may come from blanking inputs, embedded EAV and SAV codes, or signals generated internally from sync inputs. The present Application Note describes the technique of internally generating blank signals from sync inputs. For more complete and general application information, please refer to the EVD1000/1500 Data Sheet.

Detailed Operational Description

In this mode of operation, horizontal and vertical synchronization is applied on the HSYNC_IN and VSYNC_IN inputs. The chip calculates internal horizontal blanking, vertical blanking and field signals from the sync inputs. HBLNK_OUT, VBLNK_OUT, HSYNC_OUT, and VSYNC_OUT signals come from the chip synchronized to the output data.

As described in the Data Sheet, if BLNK_SRC and the BLNK_SRC_RST register are configured properly, the chip will generate internal blanking signals from the sync inputs in one of two manners as described below.

If RT_FORCE.FORCE is set to 0 then the chip will attempt to match the sync inputs to one of the standards in the following list. If successful it will generate appropriate blanking signals and will synchronize properly. If it is unsuccessful in matching to one of the standards in the list then synchronization will not occur and output will not be generated.

SMPTE Standard	260M	274M	274M	267M	293M	295M	295M	296M
Name	1035I60	1080P60	1080I60	480I60	483P60	1080P50	1080I50	720P60
Vertical Frequency	60	60	60	59.94	59.94	50	50	60
Dot Clock (Mhz)	74.25	148.5	74.25	13.5	27	148.5	74.25	74.25
Horizontal Pixels	2200	2200	2200	858	858	2376	2376	1650
Horizontal Active Pixels	1920	1920	1920	720	720	1920	1920	1280
Horizontal Blank Pixels	280	280	280	138	138	456	456	370
Horizontal Front Porch Pixels	44	44	44	16	16	81	81	70
Horizontal Sync Pixels	44	44	44	63	63	66	66	40
Horizontal Back Porch Pixels	192	192	192	59	59	309	309	260
Vertical lines/frame	1125	1125	1125	525	525	1250	1250	750
Vertical Active Lines/frame	1035	1080	1080	480	483	1080	1080	720



If RT_FORCE.FORCE is set to 1 then the chip will assume that the registers described in the table below describe the input raster format and blanks will be generated appropriately.

Serial Configuration Registers	Description
{RT_LAST_PIXEL_HBLNK[11:8], RT_LAST_PIXEL_HBLNK[7:0]}	Number of pixels between the leading edge of horizontal sync and the trailing edge of horizontal blank
{RT_LAST_PIXEL_HACTIVE[11:8], RT_LAST_PIXEL_HACTIVE[7:0]}	Number of pixels between the leading edge of horizontal sync and the leading edge of horizontal blank in the next line
{RT_HBLNK_PIXELS[11:8], RT_HBLNK_PIXELS[7:0]}	Number of pixels during horizontal blanking time
{RT_LAST_LINE_VBLNK1[11:8], RT_LAST_LINE_VBLNK1[7:0]}	Number of lines between the leading edge of VSYNC in field #1 and the trailing edge of VBLANK in field #1
{RT_LAST_LINE_VACTIVE1[11:8], RT_LAST_LINE_VACTIVE1[7:0]}	Number of lines between the leading edge of VSYNC in field #1 and the leading edge of VBLANK near the end of field #1
{RT_LAST_LINE_VBLNK2[11:8], RT_LAST_LINE_VBLNK2[7:0]}	Number of lines between the leading edge of VSYNC in field #1 and the trailing edge of VBLANK in field #2, (only used in interlaced formats)
{RT_LAST_LINE_VACTIVE2[11:8], RT_LAST_LINE_VACTIVE2[7:0]}	Number of lines between the leading edge of VSYNC in field #1 and the leading edge of VBLANK near the end of field #2, (only used in interlaced formats)
RT_INTERLACED.INT	0 if progressive, 1 if interlaced
RT_TOP_FIELD.TOP	0 if top field is field #1, 1 if top field is field #2, (only used in interlaced formats)
RT_V_SYNC_CODE.V_SYNC_CODE	See below

V_SYNC_CODE is a 3-bit number with each bit describing the state of VSYNC at different points during the horizontal line at the beginning of a frame.

Bit	Description
V_SYNC_CODE[2]	1 if VSYNC is active $\frac{1}{4}$ of the way through the first horizontal line of a frame
V_SYNC_CODE[1]	1 if VSYNC is active $\frac{1}{2}$ of the way through the first horizontal line of a frame
V_SYNC_CODE[0]	1 if VSYNC is active $\frac{3}{4}$ of the way through the first horizontal line of a frame

In interlaced formats, the beginning of a frame is the beginning of field #1 of the frame.

For further questions or clarifications, contact your sales representative or the factory for additional support.

Enhanced Video Devices, Inc.
9830 Summers Ridge Road
San Diego, CA 92121
858-530-0100

www.enhancedvideodevices.com

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