



AN105 – EVD1000/1500 Circuit Example: YCrCb 4:4:4 Input/Output

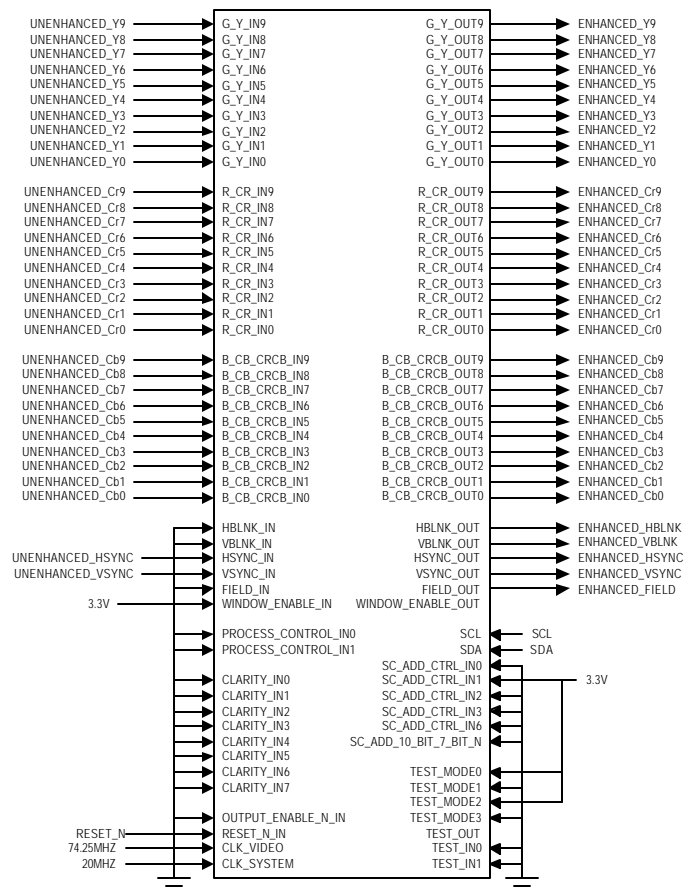
INTRODUCTION

The EVD1000/1500 has a very flexible digital I/O structure, and in-circuit applications can be configured in a variety of fashions, utilizing different video data formats, levels of user control, etc. In this series of Application Notes, a number of examples are presented, each of which includes a complete set of schematic connections as required for operation in that particular example mode. For more complete and general application information, please refer to the EVD1000/1500 Data Sheet. The present Application Note describes the method of connection for an application involving YCrCb video data input and output in 4:4:4 format, such as might be used, for example, in a higher quality 1080i HDTV system, using a microprocessor for control and, in this case, using sync rather than blanking signals.

Typical application – YCbCr 4:4:4 Input/Output

The diagram shows a typical high-definition application. The application enhances 1080i YCrCb 4:4:4 format video so all three input and output data busses are used. Unenhanced Y data is wired to the G_Y_IN bus, unenhanced Cr data is wired to the R_CR_IN bus, and unenhanced Cb data is wired to the B_CB_CRCB_IN bus. A similar wiring scheme is used for the output busses containing enhanced Y, Cr, and Cb data.

All input and output data is at the same rate. Horizontal and Vertical synchronization is applied on the HSYNC_IN and VSYNC_IN inputs. The chip calculates internal horizontal blanking, vertical blanking and field signals from the sync inputs. HBLNK_OUT, VBLNK_OUT, HSYNC_OUT, VSYNC_OUT, and FIELD_OUT signals come from the chip synchronized to the output Y, Cr, and Cb data. The CLK_VIDEO input is





at the pixel rate, i.e., 74.25Mhz in this example.

The Serial Configuration Bus is used in this example so pullup resistors are not required on the R_CR_OUT or B_CB_CRCB_OUT busses. All chip configuration is done through the Serial Configuration Bus. The device address is 0x24 for writing and is 0x25 for reading. The CLK_SYSTEM input must be wired to an active clock source between 20Mhz and the pixel clock rate. It is wired to a 20Mhz clock source in this example. It could be wired to the CLK_VIDEO input if the clock could be guaranteed to be present when Serial Configuration data is being written into the chip.

The PROCESS_CONTROL_IN[1:0] inputs are wired to VSS, causing the chip to enhance pixels for which WINDOW_ENABLE_IN is 1. WINDOW_ENABLE_IN is wired to 3.3V, causing the chip to enhance all pixels.

The CLARITY_IN bus is not used in this application, thus all bits of the bus are wired to VSS. Clarity is controlled through the Serial Configuration bus.

For further questions or clarifications, contact your sales representative or the factory for additional support.

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