



## AN104 – EVD1000/1500 Circuit Example: YCrCb 4:2:2 Input/Output

### INTRODUCTION

The EVD1000/1500 has a very flexible digital I/O structure, and in-circuit applications can be configured in a variety of fashions, utilizing different video data formats, levels of user control, etc. In this series of Application Notes, a number of examples are presented, each of which includes a complete set of schematic connections as required for operation in that particular example mode. For more complete and general application information, please refer to the EVD1000/1500 Data Sheet. The present Application Note describes the method of connection for an application involving YCrCb video data input and output in 4:2:2 format, such as might be used, for example, in a simple 1080i HDTV system, using a microprocessor for control and blanking signals for synchronization.

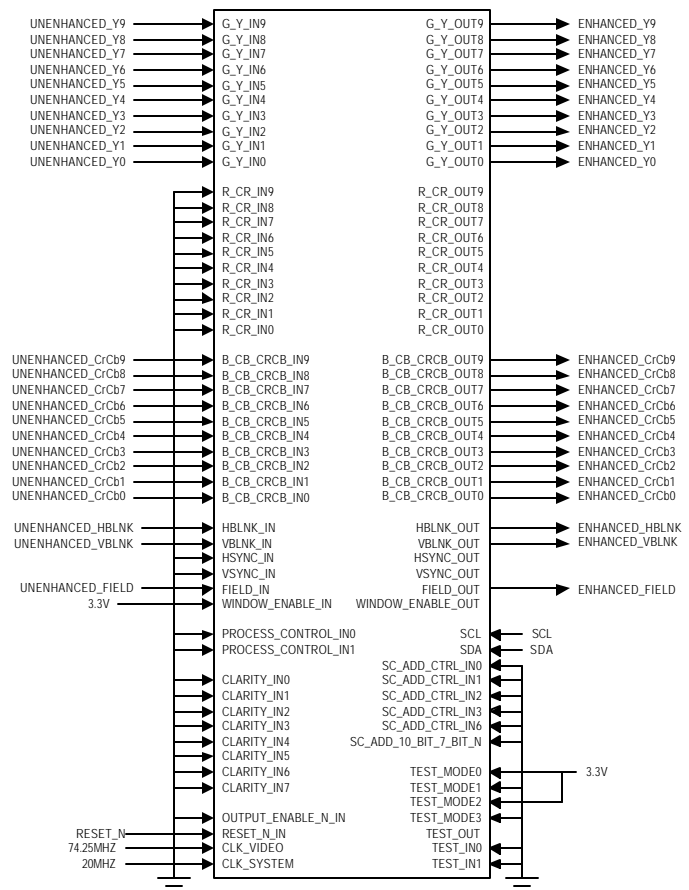
### Typical application – YCbCr 4:2:2 Input/Output

The diagram shows a typical high-definition application. The application enhances 1080i YCrCb 4:2:2 format video so two of the three input and output data busses are used.

Unenhanced Y data is wired to the G\_Y\_IN bus, unenhanced CrCb data is wired to the B\_CB\_CRCB\_IN bus, and the R\_CR\_IN bus is not used. A similar wiring scheme is used for the output busses containing enhanced Y and CrCb data.

All input and output data is at the same rate. Horizontal and Vertical timing signals are applied on the HBLNK\_IN, VBLNK\_IN and FIELD\_IN inputs. HBLNK\_OUT, VBLNK\_OUT, and FIELD\_OUT signals come from the chip synchronized to the output Y and CrCb data. The CLK\_VIDEO input is at the pixel rate, i.e., 74.25Mhz in this example.

The Serial Configuration Bus is used in this example so pullup resistors are not required on the R\_CR\_OUT or B\_CB\_CRCB\_OUT busses. All chip configuration is done through the





Serial Configuration Bus. The device address is 0x20 for writing and is 0x21 for reading. The CLK\_SYSTEM input must be wired to an active clock source between 20Mhz and the pixel clock rate. It is wired to a 20Mhz clock source in this example. It could be wired to the CLK\_VIDEO input if the clock could be guaranteed to be present when Serial Configuration data is being written into the chip.

The PROCESS\_CONTROL\_IN[1:0] inputs are wired to VSS, causing the chip to enhance pixels for which WINDOW\_ENABLE\_IN is 1. WINDOW\_ENABLE\_IN is wired to 3.3V, causing the chip to enhance all pixels.

The CLARITY\_IN bus is not used in this application, thus all bits of the bus are wired to VSS. Clarity is controlled through the Serial Configuration bus.

For further questions or clarifications, contact your sales representative or the factory for additional support.

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